1 GHz DIVIDER-BY-256

This silicon monolithic integrated circuit is an ECL fixed-ratio divide-by-256 scaler for input frequencies in the range 70 to 1000 MHz, a supply voltage of 5 or 5,2 V and an ambient temperature of 0 to + 70 °C. The inputs of the circuit are differential and internally biased to permit capacitive coupling or asymmetrical drive. For a sinusoidal input waveform the device becomes insensitive at low frequencies due to edge rate limitations. Operation down to d.c. is possible with square-wave drive. The divide-by-256 outputs are designed to interface with C-MOS and N-MOS circuits having a common V_{EE} (ground). They provide active pull-up.

Pins marked n.c. should preferably be grounded. The circuit may oscillate in the absence of an input signal, but this oscillation is suppressed by the application of an input signal within the specified range.

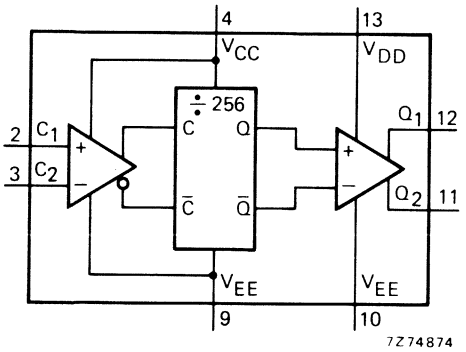

Fig. 1.

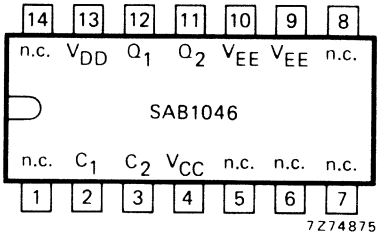

Fig. 2.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,75 to 5,46 V
	V_{DD}		4,75 to 10 V
Input frequency range	f_i		70 to 1000 MHz
Q_1 (C-MOS) output voltage			
HIGH state	V_{OH}	min.	7,5 V
LOW state	V_{OL}	max.	1,5 V
Q_2 (N-MOS) output voltage			
HIGH state	V_{OH}	min.	2,4 V
LOW state	V_{OL}	max.	0,4 V
Power consumption per package (no load)	P_{av}	typ.	320 mW
Operating ambient temperature	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

SAB1046P: 14-lead DIL; plastic (SOT-27S, T, V).

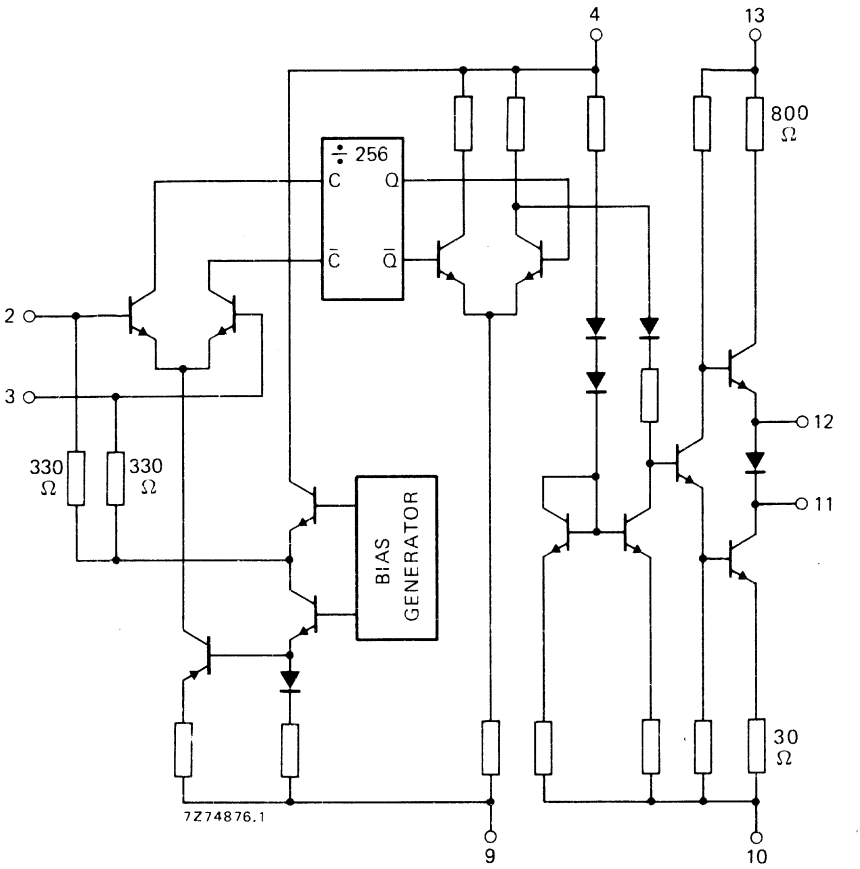

Fig. 3 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
	V_{DD}	max.	10 V
Input voltage	V_I		0 to 5,2 V
Storage temperature	T_{stg}		−55 to + 125 °C
Junction temperature	T_j	max.	125 °C

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; V_{DD} = 9 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage Q_1 (pin 12); V_{DD} = 4,75 to 10 V			
HIGH: $I_{OH} = -1\ \mu A$	V_{OH}	$V_{DD}-1,5$ V to V_{DD}	V
LOW : $I_{OL} = 1\ \mu A$	V_{OL}	0 to 1,5	V
Output voltage Q_2 (pin 11); V_{DD} = 5 V			
HIGH: $V_{CC} = V_{DD} = 5$ V; $I_{OH} = -1\ \mu A$	V_{OH}	2,4 to 5	V
LOW : $V_{CC} = V_{DD} = 5$ V; $I_{OL} = 1\ \mu A$	V_{OL}	0 to 0,4	V
Reference voltage (pin 2 or 3)	V_{ref}	2,25 to 3	V
Supply current (pin 4) pin 2 = 0 V; pin 3 = open	I_{CC}	typ. 65	mA
		< 85	mA
Supply current (pin 13)	I_{DD}	typ. 3	mA
		< 5	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 4,75 to 5,46 V; V_{DD} = 4,75 to 10 V; T_{amb} = 0 to 70 °C.

	symbol	pin under test	min.	typ.	max.		conditions
Input frequency	f_i		70	–	1000	MHz	sinusoidal input voltage $V_{i(p-p)}$ = 600 mV; * tested frequency on pin 11 or 12 is $f_i/256$
Differential input voltage	$\lvert V_2-V_3 \rvert_{p-p}$	2 and 3	–	–	1,4	V	
Slew rate for operation: down to 70 MHz			80	–	–	V/μs	square-wave drive $V_{i(p-p)}$ min. 160 mV *

Guaranteed operating region (see also Fig. 4)

		input frequency				
	MHz	70	200	500	900	1000
Minimum required input level $V_{i(p-p)}$ *	mV	355	160	140	100	200
	dBm	−5	−12	−13	−16	−10

* For definition of input voltage see Fig. 5.

A.C. CHARACTERISTICS (continued)

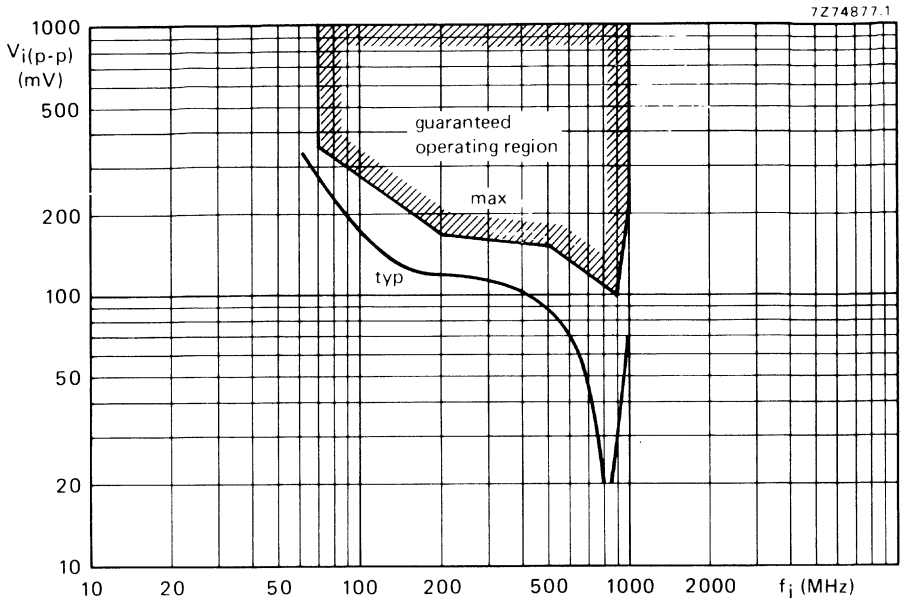

Fig. 4 V_{CC} = 5 V; V_{DD} = 5 to 9 V; T_{amb} = 0 to 70 °C.

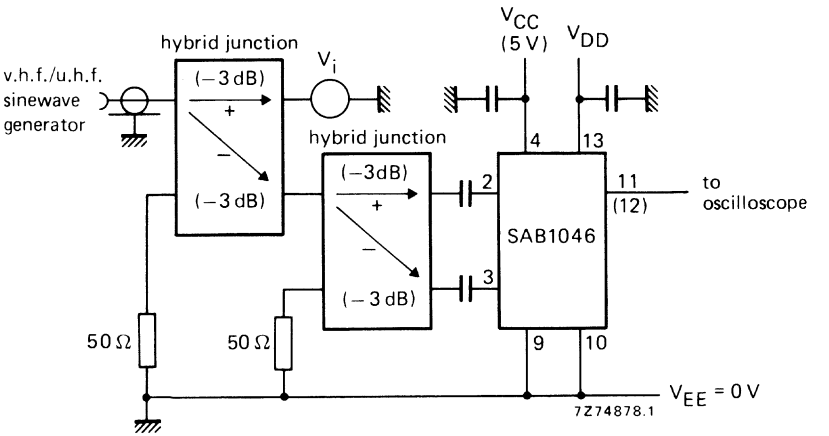

Fig. 5 Test circuit.

- Cable must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device must be kept short.
- Hybrid junctions are ANZAC H-183-4 or similar.

APPLICATION INFORMATION

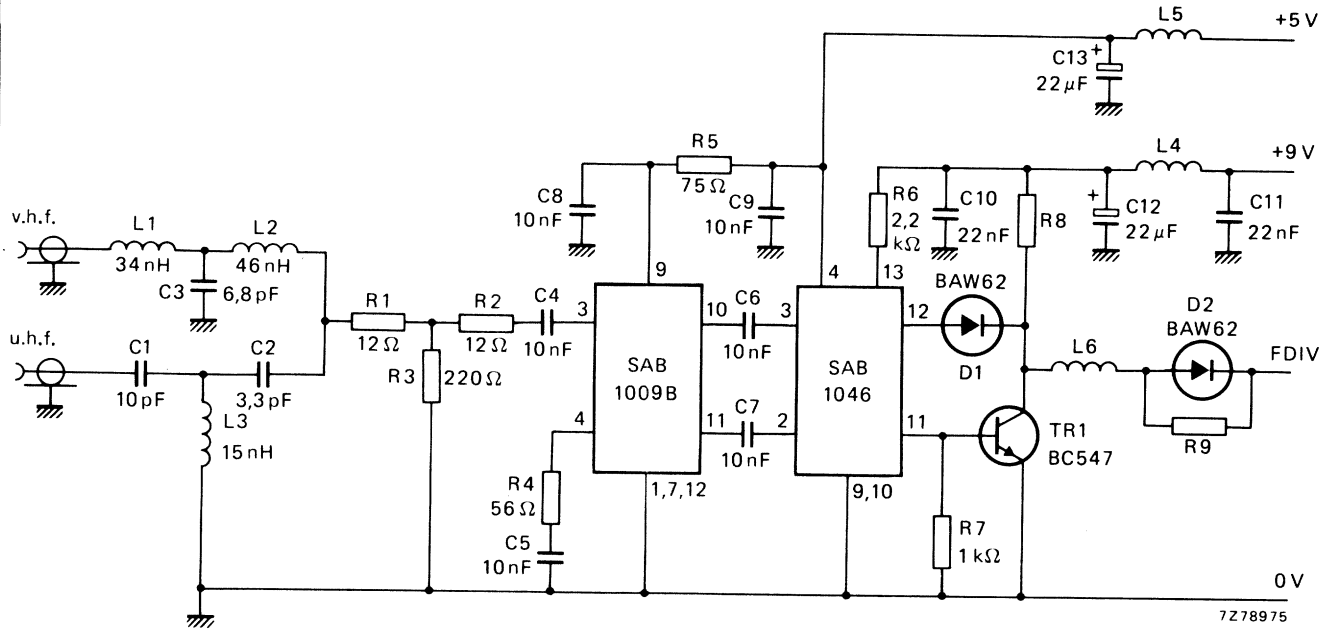

Fig. 6 H.F. divider for DICS in television receivers (prescaler module).

Values of R8, R9 and L6 have to be chosen in accordance with the load capacitance. The pins not mentioned are connected to ground except pin 5 of SAB1046 which is connected to V_{CC}.

APPLICATION INFORMATION (continued)

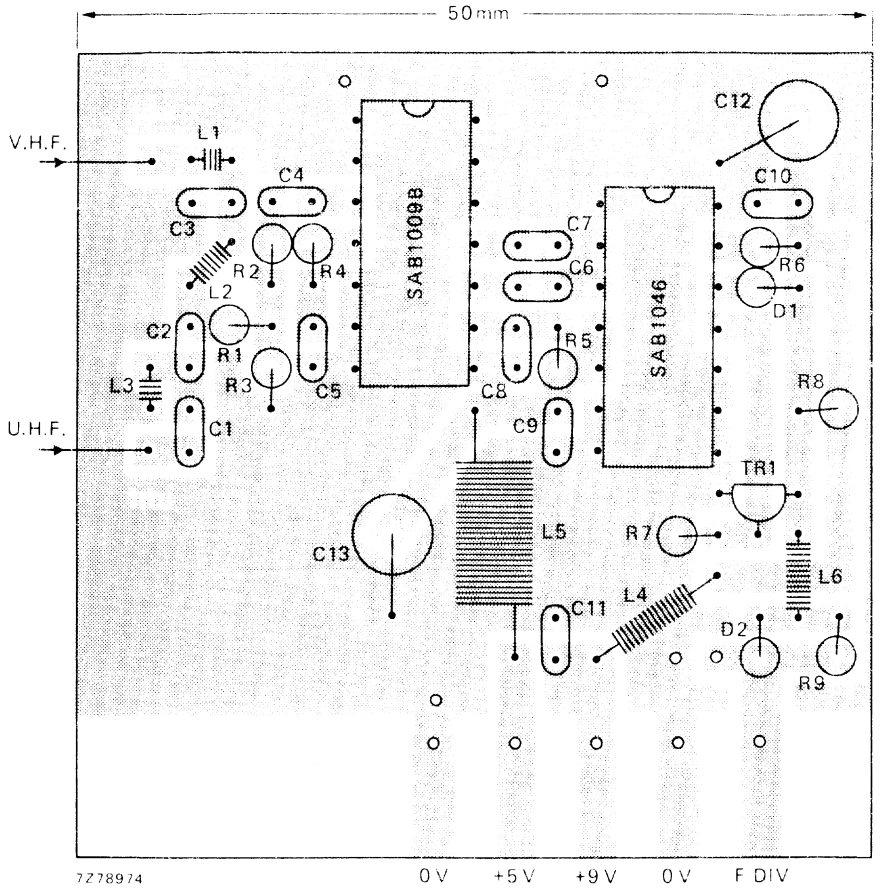

Fig. 7 Component layout of circuit shown in Fig. 6.